REMARKS

A colon has been inserted into claim 7 as suggested by the Examiner.

Applicants agree with the Examiner that the phase in claims 7 and 17 is unnecessary. It has been deleted from claim 7 and claim 17 has been cancelled. Accordingly, the rejection under 35 U.S.C. 112, second paragraph, is moot.

The rejection of claims 7, 14-18 and 24-26 under 35 U.S.C. 102 over Tsukamoto is respectfully traversed.

The independent claim 7 calls for a stepped impedance structured resonator which is a laminate having a set of three layers, the middle layer being a dielectric. Each outer layers includes a pair of spaced areas which are non-conductive areas and a conductive area between the non-conductive areas. The two outer layers are positioned such that a portion of each non-conductive area in one outer layer overlaps a portion of the corresponding non-conductive area in the other outer layer in the lamination direction. The juxtaposition of two non-conductive areas with dielectric between them results in the formation of an inductive area. In addition, a portion of the conductive areas in the two outer layers overlap each other with the dielectric layer positioned between them to form a capacitive area. This construction is not taught (or suggested) by the Tsukamoto reference.

The dielectric filter of Tsukamoto is not a laminate having the superposed set of first, second and third layers of the claimed invention. Instead, the dielectric filter of this reference is a dielectric block in which certain surfaces have been made conductive. Since the filter is a block rather than a laminate, there is no "lamination direction". Whether the term "lamination direction" referenced in the Office Action is construed as being either up and down or side to side, the filter does not anticipate the claimed invention.

When viewed from an up and down perspective, it is possible to argue that the top of the dielectric block 1 is a "layer" but if so, there is no set of two additional layers disposed below that top surface. The rest of the filter is a unitary dielectric block containing holes whose surface has been made conductive.

When viewed from side to side, there is also no set of the designated superposed layers. The electrodes 5a-5d might broadly be considered layers, and adjacent electrodes with the dielectric between them may be considered to define a capacitive area. However, each of the electrodes is a continuous conductive layer running from the top of the projections 7a-7b to the bottoms of holes 2a-2b. As clearly shown in Figure 2, the electrode 5a of the conductive surface 3a of hole 2a are continuous and are not interrupted by any areas of non-conductivity. None of these electrodes have spaced non-conductive areas with a conductive area between them.

The Office Action characterizes elements 2a-2b as being non-conductive areas which overlap in the lamination direction. Putting aside the fact that the filter is a block and does not have a "lamination direction", and viewing the structure from a side to side perspective, holes 2a-2b do overlap each other. However, if each of the holes is considered a "layer", then the layer is completely non-conductive and there is no second non-conductive area in the layer. As previously noted, if the "lamination direction" would be considered from the top to the bottom, everything below the top is uniform and there is no intermediate layer of dielectric.

The Office Action characterizes "capacitors 7a-7c" is being made up of a superposed set of three (3) layers. Elements 7, however, are projections of the dielectric material extending above the surface of the rest of the dielectric block and are integral with the block. Electrodes designated by the numeral 5 are positioned on either side of the dielectric projection 7, are continuous and lack non-conductive areas. While the Office

Action characterizes the elements designated by the numeral 2 as being non-conductive areas, these are holes and form "layers" which are separate from the electrode layers 5 as opposed to being a part of the electrode layer.

The Office Action asserts in that Figure 1a shows non-conductive elements 2a-2b overlapping in the side direction to form inductive areas. This is not correct since each of adjacent holes 2 have a conductive area between and therefore do not form inductive areas.

The remaining members of the rejected claims are also not anticipated for the same reasons as specified above with respect to claim 7.

Claims 8-13 and 21-23 were rejected under 35 U.S.C. 103 over Tsukamoto in view of Cadho. The additional reference asserted to show a laminate containing additional layers deposed to form at least one additional superposed set of first, second and third layers. As just stated, this would be correct but the addition of the word "said" to the designation of the first, second and third layers in the Office Action makes the contention incorrect. The first and third layers of the claims are composed of a pair of non-conducting areas with a conductive area between them. Each of the lamination direction layers in Cadho is either completely a dielectric or an internal electrode. There are no pair of non-conductive areas in any of the conductive layers of this reference. Given this basic deficiency in this reference, and the very different structures in the two references suggested to be combined, the further contentions about Cadho need not be addressed here.

Claims 19 and 20 were rejected under 35 U.S.C. 103 over Tsukamoto in view of Chun. Chun is relied on only to show a shielding electrode and thus fails to cure any of the basic deficiencies in Tsukamoto. Accordingly, the combination cannot render the claimed invention obvious.

In light of the foregoing considerations, it is respectfully submitted that all rejections should be withdrawn and the application allowed.

Respectfully submitted,

Dated: December 14, 2007

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